a clock generation circuit, said clock generation circuit using a received signal to generate a clock signal and a sampling signal,

received data being the information transmitted to said IC card by way of said received signal,

said sampling signal having a plurality of pulses during each cycle of said clock signal,

a plurality of logic levels being generated during said each cycle of said clock signal,

a logic level of said plurality of logic levels being the signal level of said received signal when sampled by a pulse of said plurality of pulses; and

a decoder, said decoder decoding said plurality of logic levels to generate said received data.